

## REMARKS

Applicant requests entry of the above-identified amendment. Prosecution on the merits is respectfully requested.

In addition, Applicant also submits these additional remarks. Claims 5 and 6 include the following limitation: “at least a portion of the contact hole region and at least a portion of said first electrode are filled with a flattening layer; and said emissive element layer and said second electrode are formed above said flattening layer.” Claims 7 and 8 include the following limitation: “at least a portion of a recess of said first electrode covering said contact hole is covered by a flattening layer; and said emissive element layer is formed above said flattening layer.” Claims 9-11 include the following limitation: “at least a portion of a recess of said first electrode created due to said second contact hole is filled with a flattening layer; and said emissive layer and said second electrode are formed above said flattening layer and said first electrode.” None of the references teach or suggest those limitations.

First, Yamazaki et al. (US 6,420,200, submitted by Applicant) (“Yamazaki”) does not teach or suggest that that at least a portion of the first electrode is filled with a flattening layer or that the flattening layer covers the first electrode. This is clear from Figure 2 of Yamazaki. Instead, Yamazaki teaches that the flattening layer 44 is located below the first electrode 46 or 51. See Figures 2 and 14 of Yamazaki.

Moreover, the reason for the flattening layer 44 of Yamazaki is different than the reason for the flattening layer in claims 2 and 3. The flattening layer in claim 5-8 is present because of the contact hole. Yamazaki teaches that the reason for the flattening layer is to flatten the step caused by the thin film transistors. Column 7, lines 64-67 explain that the insulation layer 44 is formed to flatten the step, which has been caused by to the plurality of thin film transistors. As such, because the flattening layer 44 flattens the step in the thin film transistors, it must be located directly above the thin film transistors and not the first electrode.

Even when Wilson et al. (“Handbook of Multilevel Metalization for Integrated Circuits, Noyes Publ., Westwood, New Jersey (1993), pp 357, 386, and 389, submitted by Applicant) (“Wilson”) is considered along with Yamazaki, a person with ordinary skill in the art would not be motivated to fill, with a flattening layer, a recess formed above a first electrode or a wiring layer due to a contact hole. From Wilson, a person with ordinary skill in the art would understand that unevenness cannot be improved by covering a surface with

unevenness by a CVD film, but such a surface can be flattened by covering the entire surface by SOG or the like, which is common knowledge.

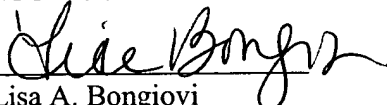
As described above, although there is a very large recess on the electrode 46 shown in Figure 2 of Yamazaki, the recess is directly covered by the EL layer 47. It is therefore clear that even in Yamazaki, which discloses a structure of an EL element, there is no recognition of the need for filling the recess formed on a first electrode due to a contact hole.

Claims 5-11 also include the following limitation: "in said element to be driven, light is emitted by supplying charges from said first and second electrodes to said emissive element layer." This limitation is not taught or suggested by the references. When a surface of the first electrode is covered by an insulating flattening layer, the covered region cannot supply charges to the emissive element layer. In the field of EL elements, in which obtaining as much emissive region as possible, that is, increasing the aperture ratio, is a high priority, a person with ordinary skill in the art would not be motivated to cover a portion of the first electrode, and thereby narrow the emissive region, even if the covered portion corresponds to a recess. Thus, no person with ordinary skill in the art would be motivated to fill a recess using a flattening layer to Yamazaki.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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